

**NEW UTILITY PATENT APPLICATION
TRANSMITTAL***(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))*Docket No.
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submission**TO THE ASSISTANT COMMISSIONER FOR PATENTS****Box Patent Application
Washington, D.C. 20231**

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

METHOD AND STRUCTURE FOR REDUCING LEAKAGE CURRENT IN CAPACITORS

and invented by:

Lingyi A. Zheng and Er-Xuan Ping

IF A CONTINUATION APPLICATION, check appropriate box and supply requisite information:☐

Continuation

☐

Divisional

☐

Continuation-in-part (CIP) of prior application No.:

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 29 pages(s) and including the following:
 - a. ☒ Descriptive title of the invention
 - b. ☐ Cross references to related applications *(if applicable)*
 - c. ☐ Statement regarding Federally-sponsored research/development *(if applicable)*
 - d. ☐ Reference to microfiche appendix *(if applicable)*
 - e. ☒ Background of the invention
 - f. ☒ Brief summary of the invention
 - g. ☒ Brief description of the drawings *(if drawings filed)*
 - h. ☒ Detailed description
 - i. ☒ Claims as classified below
 - j. ☒ Abstract of the disclosure

Application Elements (continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 U.S.C. 113)*
☒ Formal ☐ Informal Number of sheets: 5
4. ☒ Oath or Declaration
 a. ☒ Newly executed (original or copy) ☐ Unexecuted
 b. ☐ Copy from a prior application (37 C.F.R. 1.63(d) *(for continuation/divisional applications only)*)
 c. ☐ With Power of Attorney ☐ Without Power of Attorney
5. ☐ Incorporation by reference *(usable if Box 4b is checked)*
 The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer program in microfiche
7. ☐ Genetic sequence submission *(if applicable, all must be included)*
 a. ☐ Paper copy
 b. ☐ Computer readable copy
 c. ☐ Statement verifying identical paper and computer readable copies

Accompanying Application

8. ☒ Assignment papers *(cover sheet & document(s))*
9. ☐ 37 C.F.R. 3.73(b) statement *(when there is an assignee)*
10. ☐ English translation document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☐ Certified copy of priority document(s) *(if foreign priority is claimed)*
15. ☐ Certificate of Mailing
☐ First Class ☐ Express Mail (Label No.: _____)
16. ☐ Small Entity statement(s) -- # submitted _____ *(if Small Entity status claimed)*

Accompanying Application (continued)

- 17.
- ☐
- Additional enclosures (please identify below):

Fee Calculation and Transmittal

The filing fee for this utility patent application is calculated and transmitted as follows:

☒ Large Entity ☐ Small Entity

<u>CLAIMS AS FILED</u>						
For	# Filed	# Allowed			Rate	Fee
Total Claims	95	-	20	=	75	x \$18.00 \$1,350.00
Independent Claims	7	-	3	=	4	x \$78.00 \$312.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>						
Other Fees (specify purpose): Assignment Recordation						\$40.00
BASIC FEE						\$690.00
TOTAL FILING FEE						\$2,392.00

- ☒ A check in the amount of \$2,392.00 to cover the total filing fee is enclosed.
- ☒ The Commissioner is hereby authorized to charge and Deposit Account No. 4 - 1073 as described below. A duplicate copy of this sheet is enclosed.
- ☐ Charge the amount of _____ as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.31(b).



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR U.S. LETTERS PATENT

Title:

**METHOD AND STRUCTURE
FOR REDUCING LEAKAGE CURRENT IN CAPACITORS**

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METHOD AND STRUCTURE FOR REDUCING LEAKAGE CURRENT IN CAPACITORS

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FIELD OF THE INVENTION

The present invention relates to a method of forming a capacitor with reduced leakage current, and more particularly, to a method of oxidizing a capacitor dielectric layer so that leakage current across the conductive layers of the capacitor is reduced while capacitance is substantially unaffected. The invention also relates to the capacitor structures formed according to the various embodiments of the method herein set forth.

BACKGROUND OF THE INVENTION

Figure 1 illustrates a semiconductor device 110 containing a planar capacitor structure 114 formed over a substrate 112. The structure of Figure 1 is not intended to represent a particular capacitor as constructed in a semiconductor device, but is merely used as an example to illustrate the main components of such a capacitor. Substrate 112 may be formed, for example, of silicon or silicon-on-insulator (SOI) material or other well known substrate material. A first conductive layer or bottom electrode 116 is formed over the substrate using materials and methods known in the art. For example, the first conductive layer may be formed of two layers: a polysilicon bottom layer with a hemispherical silicon grain, or HSG, layer atop the polysilicon.

The capacitor structure 114 may be coupled to an active region 113 in the substrate, for example a source or drain region of a MOS transistor. Alternately, the capacitor structure 114 may be insulated from the substrate 112 through an insulating region. A capacitor dielectric layer 118 is formed over the conductive layer 116, and may be formed of a substantially nonconductive material such as, for example, silicon

nitride (Si_3N_4), or other dielectric material known in the art. A thin protective layer 119 is then formed over the dielectric layer using gaseous oxygen and hydrogen. The protective layer may thus comprise silicon dioxide (SiO_2) which forms as the oxygen reacts with the silicon from the silicon nitride in the dielectric. The protective layer serves to "heal" any defects in the dielectric layer 118 which might cause leakage problems across the resulting capacitor. A second conductive layer or top electrode 122 is formed over the protective layer and may be formed with polysilicon or other conductive material.

In order to effectively utilize the capacitor 114 in modern dynamic random access memories (DRAMs), however, it has been necessary to reduce its size and substantially minimize the thickness of the dielectric layer 118. In many embodiments, it is therefore especially desirable that the dielectric layer be less than about 60 Angstroms in thickness, and even more desirably, less than about 50 Angstroms thick. Unfortunately, leakage current between the first and second conductive layers 116, 122 tends to increase exponentially as the thickness of the dielectric layer 118 is reduced to below 50 Angstroms. While formation of the protective layer 119 has been instrumental in helping to reduce this leakage current, there is still considerable need for a further reduction to enhance overall capacitor performance, as capacitor sizes continue to shrink in memory devices.

What is therefore needed in the art is a new method of forming a capacitor structure which results in reduced leakage current, while overall capacitance is substantially unaffected. Also needed are new capacitors in which leakage current between conductive layers is minimized, while capacitance is substantially maintained.

SUMMARY OF THE INVENTION

The invention provides a method of forming a capacitor in a semiconductor device in which a first layer of conductive material is first formed, a second layer of a dielectric is formed over the first layer, the second layer is then contacted with hydrogen, oxygen and nitrous oxide gases to form an oxidation layer over the second layer, and a third layer of conductive material is then formed over the second layer. The resulting structure exhibits a lowered current leakage with little loss of capacitance when compared with similar capacitor structures in which the dielectric is built with a conventional hydrogen and oxygen treatment which forms an oxidation layer on the dielectric.

The invention further provides a method of oxidizing a capacitor dielectric by contacting it with hydrogen, oxygen and nitrous oxide gases to form an oxidation layer thereon. Other suitable gases would include those with an O (oxygen) or F (fluorine) moiety that bonds strongly to silicon.

The invention also provides a method of oxidizing a capacitor dielectric which involves adding an oxygen containing gaseous material (e.g, nitrous oxide) to a mixture of oxygen and hydrogen gases, and then contacting the capacitor dielectric with the gaseous mixture so as to form an oxidation layer over the capacitor dielectric. The thus processed dielectric has a lower leakage current than does the same dielectric having an oxidation layer formed by contacting the dielectric with only hydrogen and oxygen gases under the same reaction conditions.

The invention also provides a method of forming a capacitor dielectric over a substrate in which a layer of silicon nitride is deposited over a conductive layer which has first been formed over a substrate. The silicon nitride layer is then contacted with hydrogen, oxygen and nitrous oxide gases so as to form an oxidation layer thereon.

The invention also provides a method of oxidizing a dielectric layer of capacitor in an intermediate stage of fabrication in which the dielectric layer is exposed to a combination of hydrogen, oxygen and nitrous oxide gases, and the flow rate of the nitrous oxide gas is increased during oxidation while the flow rate of the hydrogen and oxygen gases are maintained substantially constant. The gas ratio of nitrous oxide to hydrogen and oxygen can be varied by either changing the nitrous oxide gas flow rate while keep the hydrogen and oxygen flow rates constant, or vice versa.

The invention also provides a semiconductor device having a substrate with at least one capacitor formed thereover. The capacitor includes first and second conductive layers, with a dielectric between these two layers which has been oxidized in the presence of hydrogen, oxygen, and nitrous oxide gases to produce an oxidation layer over the dielectric.

The invention further provides a memory cell of a semiconductor device which includes a container capacitor. The capacitor has first and second conductive layers, a dielectric layer between the conductive layers and an oxidation layer over the dielectric layer. The oxidation layer is formed by an oxidation of the dielectric layer in the presence of a combination of hydrogen, oxygen and nitrous oxide gases.

The invention further provides an integrated circuit which includes at least one capacitor formed over a substrate, wherein the capacitor contains a first conductive layer, a dielectric layer over the conductive layer, an oxidation layer over the dielectric layer, and a second conductive layer over the dielectric layer. The oxidation layer is formed by an oxidation of the dielectric layer in the presence of a combination of hydrogen, oxygen and nitrous oxide gases.

The invention also provides a processor based system which includes a processor, and an integrated circuit device coupled to the processor. At least one of the processor and the integrated circuit device contains a capacitor which includes first and

second conductive layers, a dielectric layer between the conductive layers and an oxidation layer over the dielectric layer. The oxidation layer is formed by an oxidation of the dielectric layer in the presence of a combination of hydrogen, oxygen and nitrous oxide gases.

5 These and other advantages and features of the present invention will become more readily apparent from the following detailed description and drawings which illustrate various exemplary embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

10 Figure 1 is a cross sectional view of a conventional planar capacitor.

 Figure 2A is a cross sectional view of a semiconductor device showing a capacitor in an intermediate stage of fabrication according to one exemplary embodiment of the invention.

15 Figure 2B is a cross sectional view of the device shown in Figure 2A in a further stage of fabrication.

 Figure 2C is a cross sectional view of the device shown in Figure 2B in a further stage of fabrication.

 Figure 3 is a cross sectional view of a capacitor structure according to a further exemplary embodiment of the invention.

20 Figure 4 is a leakage current vs. voltage plot (I-V plot) as measured for various capacitors with a cell dielectric at 47 Angstroms after various oxidation processes according to various exemplary embodiments of the invention.

 Figure 5 is a leakage current vs. voltage plot (I-V plot) as measured for various capacitors with a cell dielectric at 59 Angstroms after various oxidation processes
25 according to various exemplary embodiments of the invention.

Figure 6 is a leakage current vs. capacitance plot as measured for the capacitors of Figures 4 and 5, with 47 Angstrom and 59 Angstrom dielectric layers respectively, after oxidation processes according to various exemplary embodiments of the invention.

5 Figure 7 is a block diagram of a typical processor based system which includes integrated circuits that utilize capacitors constructed in accordance with exemplary embodiments of the present invention.

10 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention in its broadest embodiment is directed to a method of fabricating a capacitor for use in a semiconductor device in which leakage current across conductive layers is reduced, while overall capacitance is substantially maintained.

15 Reference herein shall be made to the term "substrate," which is to be understood as including silicon, a silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) structures, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. In addition, when reference is made to a "substrate" in the following description, previous
20 process steps may have been utilized to form arrays, regions or junctions in or over the base semiconductor structure or foundation. In addition, the semiconductor need not be silicon-based, but could be based on silicon-germanium, germanium, indium phosphide, or gallium arsenide. The term "substrate" as used herein may also refer to any type of generic base or foundation structure.

25 Referring again to the drawings in which like numerals indicate like components throughout the various embodiments, Figure 2A shows a planar capacitor

214 formed over a substrate 212 in a semiconductor device 210 in an intermediate stage of fabrication. Also shown in Figure 2A are a first conductive layer 216 and a dielectric layer 218. For purpose of simplification, it will be assumed that planar capacitor 214 connects with an active region 113 in substrate 212, though this is not necessary to the invention. The first conductive layer 216 is formed of one or more conductive materials, for example, a layer of polysilicon over a layer of HSG, both of which may be deposited over region 113 using silane (SiH_4) gas via a chemical vapor deposition (CVD) or low pressure chemical vapor deposition (LPCVD) process at moderate temperature of about 500 to 600°C, or other known process in the art. The thickness of the first conductive layer is typically within the range of about a few Angstroms to several hundred Angstroms. Thereafter, the dielectric layer 218 is formed of a substantially non-conductive material such as, for example, silicon nitride (Si_3H_4). The silicon nitride dielectric layer 218 may be deposited using dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) gases using LPCVD. It is preferred that the dielectric layer 218 be relatively thin as compared to the conductive layer 216. More desirably, the dielectric layer 218 should not exceed about 60 Angstroms in thickness. It is even more preferred that the dielectric layer not exceed about 50 Angstroms in thickness. In certain embodiments, a dielectric layer which is between about 40 to 50 Angstroms in thickness, more preferably between about 45 to 50 Angstroms, may be especially desirable. The dielectric layer serves as an insulator between the first conductive layer 216 and the second conductive layer 222, hereinafter defined. While it is desirable that the dielectric layer not be too thick, it is also preferred that this layer not be too thin, as it may not then be a strong enough insulator to stop charges from passing between the first and second conductive layers.

Referring now to Figure 2B, an oxidation layer 220 is next formed over the dielectric layer 218. As used herein, the term "oxidation" is used to denote an initial

oxidation of the dielectric layer, or may be used to denote an oxidation of the dielectric layer which occurs after previous oxidation of the dielectric layer has occurred. The oxidation layer will serve to repair or heal any defects in the dielectric layer 218. These defects may take the form of "pinholes" or other openings in the dielectric layer, which if left untended, could reduce the effectiveness of the dielectric layer by allowing charges to pass through. The oxidation layer is formed of an insulative material, e.g an oxide, which effectively plugs the pinholes in the dielectric layer 218.

To form the oxidation layer 220, the dielectric layer 218 is contacted with a combination of gases. These include hydrogen, oxygen and nitrous oxide (N_2O) gases.

Reaction of the hydrogen, oxygen and nitrous oxide gases typically takes place in an atmospheric furnace at a temperature within the range of about 600 to 1000°C, with about 700 to 800°C being preferred. The flow rates for each of the reaction gases are within the range of about 1 to 15 standard-liters/minute (slm), more desirably about 2 to 10 slm. Preferably, the gases are introduced together into the atmospheric furnace.

The oxidation layer is grown over the dielectric layer so as to be relatively thin, and preferably is less than about 5 Angstroms, and more preferably less than about 3 Angstroms.

In a preferred embodiment of the invention, the flow rate for the nitrous oxide gas is at least about 0.5 slm, more preferably about 2.5 slm, and is even more preferably at least about 5 slm. For some dielectric layers, it may be desirable to have a flow rate for the nitrous oxide of at least about 10 slm. It has now been discovered that as the flow rate of nitrous oxide introduction is increased, leakage current is reduced, even as all other reaction parameters are kept substantially constant. Even more desirably, the flow rates of hydrogen and oxygen gas introduction are maintained constant at a rate within the range of about 4 to 8 slm, with about 5 to 7 slm being more preferred while the flow rate of the nitrous oxide gas is increased during the

oxidation period. In some embodiments, the flow rate of the nitrous oxide will be within the range of about .05 to about 1.7 times that of the respective flow rates for hydrogen and oxygen.

Referring now to Figure 2C, after oxidation of the dielectric layer 218 to form oxidation layer 220 a second conductive layer 222 is formed over the oxidation layer 220. The second conductive layer forms the upper electrode or cell plate of the capacitor 214. The second conductive layer is deposited using a conductive material and may comprise, for example, doped polycrystalline silicon, or polysilicon for short. The second conductive layer of polysilicon may be formed using silane gas to deposit the polysilicon. Preferably, deposition takes place using a CVD or LPCVD process. The thickness of the second conductive layer can vary from about a few Angstroms to several hundred Angstroms as needed for a particular environment of use.

It is to be understood that the shape of the formed capacitor 214 shown in Figure 2C is for purposes of illustration only. Those skilled in the art will recognize that any suitable shape is within the scope of the invention, and therefore the capacitor may be a planar, curved or container capacitor, or have other configuration, and may have a cross-sectional shape of a square, rectangle, oval, trapezoid, parallelogram, or other any other suitable shape, for example.

It is now been found that the capacitor 214 formed with the oxidation layer 220 using a combination of hydrogen, oxygen and nitrous oxide gases as heretofore set forth exhibits substantially reduced leakage current. For example, the leakage current as measured at -1.6 Volts for a thickness of dielectric layer (which is less than or equal to 59 Angstroms) is less than about -3.00 E^{-08} , and preferably is less than about -2.50 E^{-08} . It is especially preferred that the leakage current be less than about -2.00 E^{-08} .

The capacitor 214 of the invention exhibits substantially reduced leakage current as compared to a capacitor having an identical structure except that the

oxidation layer is formed under the same reaction conditions using only hydrogen and oxygen gases. Thus, it is within the scope of the invention that leakage current of the resulting capacitor can be reduced by at least about 30% and more desirably by at least about 40% as compared to a capacitor formed with an oxidation layer formed using only hydrogen and oxygen gases. In a more preferred embodiment, reduction of leakage current can be at least about 50%.

The aforesaid reduction in leakage current occurs while capacitance of the formed capacitor 214 is substantially unaffected. As used herein, the term “substantially unaffected” means that any change in capacitance does not exceed about 10%. Once again, the standard for comparison is a capacitor having a dielectric layer which is formed using hydrogen and oxygen gases only (with no nitrous oxide) using the same process conditions and having the same structural configuration.

The capacitors formed according to the various embodiments of the invention should have a capacitance which is at least about 20.00 fF/ μm^2 as measured at -1.6 volts for a 47 Angstrom thick dielectric layer.

While not wishing to be bound by any particular theory, it appears that the oxidation layer 220 formed from the combination of hydrogen, oxygen and nitrous oxide gases more effectively seals the pinholes and cures other defects present in the dielectric layer 220 than does a layer formed using hydrogen and oxygen alone under the same reaction conditions. Atomic oxygen (O) might be more effective than molecular oxygen (O_2) in this regard, and may reduce the Si, N or other dangling bonds which generally cause defects in the dielectric layer 220. It is perhaps the combination of hydrogen, oxygen and nitrous oxide which generates/liberates more atomic oxygen than does the combination of hydrogen and oxygen gases alone.

Therefore, it is certainly within the scope of the invention to utilize other chemical compounds or materials which together with hydrogen and oxygen gases may

effectively liberate more atomic oxygen than could otherwise be generated using hydrogen and oxygen alone. The invention therefore also comprises utilization of an atomic oxygen-generating material in conjunction with oxygen and hydrogen gases in the method as heretofore described.

5 Referring now to Figure 3, there is illustrated a further embodiment of the invention. Shown is a more traditional container capacitor structure 314 formed as part of a memory cell of a memory device 310. The capacitor structure 314 is formed in an insulator layer 324 which in turn is formed of any suitable insulating material such as silicon dioxide, or more preferably Boro-Phospho-Silicate Glass (BPSG). A conductive
10 plug 330 formed in a contact opening 332 between a pair of gate stacks 334 provides access for the capacitor 314 to a memory cell access transistor source/drain region 336 in the substrate 312. Capacitor 314 in Figure 3 is shown with a first conductive layer 316 formed within an opening 332 in insulating layer 324 over the substrate 312, a thin dielectric layer 318 formed over the first conductive layer 316, an oxidation layer 320
15 formed as described above over the dielectric layer 318, and the second conductive layer 322 formed over the oxidation layer 320. If desired, one or more of the capacitor components may be initially formed to extend over the insulator material 324 outside of the contact opening 332, and may be subsequently planarized using etch back or chemical mechanical planarization (CMP) techniques to the level shown in Figure 3.

20 The following examples illustrate the invention according to various embodiments, but should not be construed as limiting the scope thereof.

EXAMPLE

25 Planar capacitor structures (as illustrated in Figure 2D) were formed comprising HSG (Hemispherical Silicon Grain) as the bottom electrode or first

conductive layer 216, silicon nitride as the dielectric layer 218, and polysilicon as the top electrode or second conductive layer 222. In each group an oxidation layer 220 was also formed over the dielectric layer before the top electrode was fabricated. In the capacitors of Group 1 the oxidation layer was formed using hydrogen and oxygen gases only. For capacitors in Groups 2, 3, 4, the method of the invention was utilized incorporating nitrous oxide in the oxidation gas mixture. In each of these groups (1 through 4) some capacitors were formed with dielectric layers having a thickness of 47 Angstroms, while in others the dielectric layer thickness was 59 Angstroms. The results are shown in TABLE 1:

TABLE 1.

	Group 1 (Control)		Group 2		Group 3		Group 4	
Group label	Group 1- 47A	Group 1 59A	Group 2 47A	Group 2 59A	Group 3 47A	Group 3 59A	Group 4 47A	Group 4 59A
Cell nitride Thickness	47A	59A	47A	59A	47A	59A	47A	59A
Post oxidation process	H ₂ gas flow: 6slm O ₂ gas flow: 6slm Temperature: 750C		H ₂ gas flow: 6slm O ₂ gas flow: 6slm N ₂ O gas flow: 2.5slm Temperature: 750C		H ₂ gas flow: 6slm O ₂ gas flow: 6slm N ₂ O gas flow: 5slm Temperature: 750C		H ₂ gas flow: 6slm O ₂ gas flow: 6slm N ₂ O gas flow: 10slm Temperature: 750C	
Thickness of oxide on bare Si wafers after oxidation process*	99A		98A		98A		~104A	
Wafer number	1,5,9	13,17,21	2,6,10	14,18,22	3,7,11	15,19,23,25	4,8,12	16,20,24
*A blank Si wafer is generally used to monitor the oxidation process. The oxide thickness grown on the blank Si wafer is used to control and target the oxidation process. Thus, the thickness of the oxide on the Si monitor wafer is matched to about 100 A here. Other monitor oxide thicknesses are certainly feasible, depending on the applications.								

TABLE 2 shows a comparison of electrical data for the formed capacitors

listed in TABLE 1:

TABLE 2.

	Group 1		Group 2		Group 3		Group 4	
Group label	Group 1- 47A	Group 1 59A	Group 2 47A	Group 2 59A	Group 3 47A	Group 3 59A	Group 4 47A	Group 4 59A
Capacitance (fF/ μm^2)	21.08	17.82	20.95	17.44	20.69	16.39	20.61	17.35
Leakage at -1.6V (A/ cm^2)	-4.46E-08	-3.08E-09	-2.05E-08	-2.68E-09	-1.88E-08	-2.58E-09	-1.64E-08	-2.68E-09
Capacitance refer to group 1	1	1	0.99	0.98	0.98	0.92	0.98	0.97
Leakage refer to group 1	1	1	0.46	0.87	0.42	0.84	0.37	0.87

From TABLE 2, it can be seen that the capacitors in Groups 2 through 4 have significantly reduced leakage current as compared to the capacitors of Group 1 formed using the conventional oxidation process. In addition, the leakage current data which is obtained is better for the capacitors with a 47 Angstrom dielectric layer than for capacitors with a 59 Angstrom layer. Overall, leakage current for the capacitors of Group 1 is reduced by 54 – 63%, while capacitance is reduced by only 1 – 2%. The capacitors of Groups 2 – 4 also display leakage current which is not in excess of -3.08 E^{-08} . In particular, the leakage current for the capacitors with a 47 Angstrom dielectric layer is not in excess of -2.05 E^{-08} .

The performance results are shown plotted in Figures 4, 5 and 6 (the numbers in the insets represent the wafer numbers from TABLE 1). In Figure 4, the capacitors of Group 1 (with a 47 Angstrom dielectric layer) show a significant amount of leakage current throughout a range of voltages (as indicated by the two lower plotted lines; the plots for wafers 5 and 9 have overlapped in Figure 4) than do the capacitors of the invention from Groups 2, 3, and 4. Similar, although not as pronounced, results are shown in Figure 5 where the three lower descending plots represent the wafers 13, 17

and 21 of Group 1. In Figure 6, capacitance performance has been plotted against leakage current. It is observed that the capacitance of the wafers of Groups 2, 3 and 4 is substantially unaffected (across the x axis) while leakage current is substantially improved, i.e. is less negative in the y direction, as compared to the wafers of Group 1.

5 Due at least in part to their improved electrical characteristics, the capacitors herein described have wide applicability in the semiconductor industry. A typical processor system which includes integrated circuits that utilize one or more of the capacitors formed in accordance with the present invention is illustrated generally at 700 in Fig. 7. A processor system, such as a computer system, for example, generally
10 comprises a central processing unit (CPU) 710, for example, a microprocessor, that communicates with one or more input/output (I/O) devices 740, and a hard drive 750 over a bus system 770 which may include one or more busses and/or bus bridges. The computer system 700 also includes a hard disk drive 720, a floppy disk drive 730, a random access memory (RAM) 760, a read only memory (ROM) 780 and, in the case of
15 a computer system may include other peripheral devices such as a compact disk (CD) ROM drive 730 which also communicate with CPU 710 over the bus 770. The invention may be used to produce capacitors in one or more of the processor, RAM and ROM, or a chip containing a processor and embedded memory. While Fig. 7 shows one exemplary computer system architecture, many others are also possible.

20 The foregoing description is illustrative of exemplary embodiments which achieve the objects, features and advantages of the present invention. It should be apparent that many changes, modifications, substitutions may be made to the described embodiments without departing from the spirit or scope of the invention. The
25 invention is not to be considered as limited by the foregoing description or embodiments, but is only limited by the construed scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the
United States is:

CLAIMS:

1. A method of forming a capacitor on a substrate in a semiconductor device, comprising:
 - forming a first layer of a conductive material over said substrate;
 - forming a second layer of a dielectric over said first layer;
 - contacting said second layer with hydrogen, oxygen and nitrous oxide gases so as to form an oxidation layer over said second layer; and
 - forming a third layer of conductive material over said second layer.
2. The method of claim 1, wherein said second layer is formed to a thickness not exceeding about 60 Angstroms.
3. The method of claim 1, wherein said second layer is formed to a thickness not exceeding about 50 Angstroms.
4. The method of claim 3, wherein said second layer is formed to a thickness within the range of about 45 to 50 Angstroms.
5. The method of claim 1, wherein the ratio of nitrous oxide to oxygen and hydrogen respectively is in the range of about .05 to about 1.7.
6. The method of claim 5, wherein said contacting is performed with a gas flow rate of at least about 0.5 slm for said nitrous oxide.

7. The method of claim 6, wherein said contacting is performed with a gas flow rate of at least about 2.5 slm for said nitrous oxide.

8. The method of claim 7, wherein said contacting is performed with a gas flow rate of at least about 5 slm for said nitrous oxide.

9. The method of claim 1, wherein said contacting is performed at a temperature within the range of about 600 to 1000°C.

10. The method of claim 9, wherein said contacting is performed at a temperature within the range of about 700 to 900 °C.

11. The method of claim 10, wherein said contacting is performed at a temperature within the range of about 700 to 800 °C.

12. The method of claim 1, wherein said oxidation layer is formed so as to be thinner than said dielectric layer.

13. The method of claim 12, wherein said oxidation layer is formed to a thickness less than about 5 Angstroms.

14. The method of claim 12, wherein said oxidation layer is formed to a thickness less than about 3 Angstroms.

15. The method of claim 1, wherein said contacting is performed is performed with a gas flow rate within the range of about 1 to 15 slm for each of said hydrogen, oxygen and nitrous oxide gases.

16. The method of claim 15, wherein said contacting is performed with a gas flow rate within the range of about 2 to 10 slm for each of said hydrogen, oxygen and nitrous oxide gases.

17. The method of claim 16, wherein said contacting is performed at a temperature within the range of about 600 to 1000°C.

18. The method of claim 17, wherein said contacting is performed at a gas flow rate for said oxygen which is within the range of about 4 to 8 slm.

19. The method of claim 18, wherein said contacting is performed at a gas flow rate for said hydrogen which is within the range of about 4 to 8 slm.

20. The method of claim 19, wherein said contacting is performed at a gas flow rate within the range of about 4 to 8 slm for each of said oxygen and hydrogen.

21. The method of claim 17, wherein said contacting is performed at a gas flow rate within the range of about 2.5 to 10 slm.

22. The method of claim 21, wherein said contacting is performed at a gas flow rate within the range of about 6 to 10 slm.

23. The method of claim 17, wherein said contacting is performed at a temperature within the range of about 700 to 800°C.

24. The method of claim 23, wherein said contacting is performed at a temperature of about 750°C.

25. The method of claim 23, wherein said contacting is performed at a gas flow rate for said hydrogen of about 6 slm.

26. The method of claim 25, wherein said contacting is performed at a gas flow rate for said oxygen of about 6 slm.

27. The method of claim 25, wherein said contacting is performed at a gas flow rate for said nitrous oxide of about 2.5 slm.

28. The method of claim 23, wherein said contacting is performed at a gas flow rate for said nitrous oxide of about 5 slm.

29. The method of claim 23, wherein said contacting is performed at a gas flow rate for said nitrous oxide of about 10 slm.

30. The method of claim 24, wherein said contacting is performed at a gas flow of about 6 slm for said hydrogen, about 6 slm for said oxygen, and about 2.5 slm for said nitrous oxide.

31. The method of claim 24, wherein said contacting is performed at a gas flow rate of about 6 slm for said hydrogen, about 6 slm for said oxygen, and about 5 slm for said nitrous oxide.

32. The method of claim 24, wherein said contacting is performed at a gas flow rate of about 6 slm for said hydrogen, about 6 slm for said oxygen, and about 10 slm for said nitrous oxide.

33. The method of claim 24, wherein said contacting is performed at a gas flow rate of about 6 slm for said hydrogen, about 6 slm for said oxygen, and within the range of about 1 to 15 slm for said nitrous oxide.

34. The method of claim 33, wherein said contacting is performed at a gas flow rate of about 6 slm for said hydrogen, about 6 slm for said oxygen, and within the range of about 2 to 10 slm for said nitrous oxide.

35. The method of claim 23, wherein said second layer is formed to a thickness of about 47 Angstroms.

36. The method of claim 24, wherein said second layer is formed to a thickness of about 47 Angstroms.

37. The method of claim 34, wherein said second layer is formed to a thickness of about 47 Angstroms.

38. The method of claim 35, wherein said oxidation layer is formed to be thinner than said dielectric layer.

39. The method of claim 36, wherein said oxidation layer is formed to a thickness less than about 5 Angstroms.

40. A method of forming a capacitor structure in a semiconductor device, comprising:

depositing a layer of silicon nitride over a conductive layer formed over a substrate;

contacting said silicon nitride layer with hydrogen, oxygen and nitrous oxide gases so as to form an oxidation layer over said silicon nitride layer.

41. The method of claim 40, further comprising forming a second conductive layer over said oxidation layer.

42. The method of claim 41, wherein said second conductive layer is formed of polysilicon.

43. The method of claim 40, wherein said silicon nitride layer is deposited to a thickness not exceeding about 60 Angstroms.

44. The method of claim 43, wherein said silicon nitride layer is deposited to a thickness not exceeding about 50 Angstroms.

45. The method of claim 44, wherein said contacting is performed at a flow rate for said nitrous oxide within the range of about 1 to 10 slm.

46. The method of claim 45, wherein said contacting is performed at a flow rate for said oxygen at a flow rate within the range of about 4 to 8 slm.

47. The method of claim 46, wherein said flow rate for said nitrous oxide is greater than the flow rate for said oxygen.

48. The method of claim 47, wherein the ratio of nitrous oxide to oxygen and hydrogen respectively is in the range of about 0.05 to about 1.7..

49. The method of claim 48, wherein said flow rate for said nitrous oxide is at least greater than the flow rate for said oxygen.

50. The method of claim 40, wherein said contacting is performed at a temperature within the range of about 700 to 800°C.

51. The method of claim 50, wherein said contacting is performed at a gas flow rate for each of said hydrogen and oxygen gases which is within the range of about 4 to 8 slm.

52. The method of claim 51, wherein said contacting is performed at a gas flow rate for said nitrous oxide gas which is at least about 2.5 slm.

53. The method of claim 52, wherein said contacting is performed at a gas flow rate for said nitrous oxide which is at least about 5 slm.

54. The method of claim 53, wherein said contacting is performed at a gas flow rate for said nitrous oxide which is at least about 10 slm.

55. The method of claim 52, wherein said contacting is performed at a gas flow rate for each of said hydrogen and oxygen gases which is about 6 slm.

56. The method of claim 50, wherein said silicon nitride layer is deposited to a thickness of about 45 to 50 Angstroms.

57. The method of claim 56, wherein said oxidation layer is formed to a thickness less than about 5 Angstroms.

58. The method of claim 57, wherein said oxidation layer is formed to a thickness less than about 3 Angstroms.

59. The method of claim 50, wherein said contacting is performed at a gas flow rate of about 6 slm for each of said hydrogen and oxygen gases, and at a gas flow rate within the range of about 2.5 to 10 slm for said nitrous oxide gas.

60. A method of oxidizing a dielectric in a capacitor in an intermediate stage of fabrication comprising: exposing said dielectric to a combination of hydrogen, oxygen and nitrous oxide gases, and increasing the flow rate of said nitrous oxide gas while maintaining the flow rate of said hydrogen and oxygen gases substantially constant.

61. The method of claim 60, wherein said flow rate of said nitrous oxide gas is increased over the range of from about 2.5 slm to about 10 slm.

62. The method of claim 61, wherein said exposing is performed at a hydrogen flow rate within the range of about 5 to 7 slm.

63. The method of claim 61, wherein said exposing is performed at an oxygen flow rate within the range of about 5 to 7 slm.

64. The method of claim 60, wherein said nitrous oxide flow rate is at least about 1 ½ times greater than the flow rates of each of said hydrogen and oxygen gases.

65. A method of forming an oxidized layer on a dielectric material, which comprises exposing said dielectric material to a combination of hydrogen, oxygen and nitrous oxide gases.

66. The method of claim 65, wherein said forming is effected at a temperature within the range of about 500 to 1000 C, a flow rate for said hydrogen of about 4 to 8 slm, a flow rate for said oxygen of about 4 to 8 slm, and a flow rate for said nitrous oxide of at least about 0.5 slm.

67. The method of claim 66, wherein said forming is effected at atmospheric pressure.

68. The method of claim 67, wherein said forming is effected at a temperature within the range of about 700 to 800°C.

69. The method of claim 68, wherein said forming is effected at a flow rate for said nitrous oxide of at least about 5 slm.

70. The method of claim 69, wherein said forming is effected at a flow rate for said nitrous oxide of at least about 10 slm.

71. The method of claim 67, wherein said oxidized layer is formed to a thickness less than that of said dielectric material.

72. The method of claim 71, wherein said oxidized layer is formed to a thickness less than about 5 Angstroms.

73. The method of claim 71, wherein said oxidized layer is formed to a thickness less than about 3 Angstroms.

74. The method of claim 73, wherein said flow rate for said nitrous oxide is about 0.05 to about 1.7 times the flow rate for each of said hydrogen and oxygen gases.

75. The method of claim 74, wherein said flow rate for said nitrous oxide is at least greater than the flow rate for each of said hydrogen and oxygen gases.

76. A semiconductor device, comprising:

a substrate;

a capacitor formed over said substrate, said capacitor including:
first and second conductive layers;
a capacitor dielectric formed between said first and second conductive layers;
said dielectric including an oxidation layer formed by an oxidation of said dielectric in the presence of hydrogen, oxygen and nitrous oxide gases.

77. The device of claim 76, wherein said dielectric is not greater than about 60 Angstroms in thickness.

78. The device of claim 77, wherein said dielectric is not greater than about 50 Angstroms in thickness.

79. The device of claim 78, wherein said dielectric is between 45 – 50 Angstroms in thickness.

80. The device of claim 78, wherein said semiconductor device is a memory device.

81. A processor based system comprising:
a processor; and
an integrated circuit device coupled to said processor, at least one of said processor and integrated circuit device containing a capacitor comprising:
first and second conductive layers, a dielectric layer between said conductive layers and an oxidation layer over said dielectric layer, said oxidation layer

being formed by an oxidation of said dielectric layer in the presence of a combination of hydrogen, oxygen and nitrous oxide gases.

82. The system of claim 81, wherein said first and second conductive layers are formed of polysilicon.

83. The system of claim 82, wherein said oxidation layer is less than about 5 Angstroms in thickness.

84. The system of claim 83, wherein said dielectric layer does not exceed about 50 Angstroms in thickness.

85. The system of claim 84, wherein each of said layers is formed over a substrate.

86. A memory cell of a semiconductor memory device, comprising:

a capacitor; said capacitor including first and second conductive layers, a dielectric layer between said conductive layers and an oxidation layer over said dielectric layer, said oxidation layer being formed by an oxidation of said dielectric layer in the presence of a combination of hydrogen, oxygen and nitrous oxide gases; and an access transistor for accessing said capacitor.

87. A memory cell of claim 83, wherein said capacitor is a container capacitor.

88. A memory cell of claim 87, wherein said dielectric layer is comprised of silicon nitride.

89. A memory cell of claim 88, wherein said dielectric layer is less than about 50 Angstroms in thickness.

90. A memory cell of claim 89, wherein said dielectric layer is thinner than said first conductive layer.

91. A memory cell of claim 90, wherein said first and second conductive layers are comprised of polysilicon.

92. A memory cell of claim 86, wherein said capacitor is formed in an opening in an insulative layer.

93. A memory cell of claim 92, wherein said access transistor comprises a conductive plug formed in a contact opening.

94. A memory cell of claim 93, wherein said conductive plug is formed between a pair of gate stacks.

95. A memory cell of claim 94, wherein said access transistor provides access to a source/drain region formed in a substrate.

ABSTRACT

A method of forming a capacitor with reduced leakage current on a substrate in a semiconductor device is set forth. A first layer of a conductive material is formed over the substrate, and a second layer of a dielectric is formed over the first layer.

- 5 The second layer is contacted with hydrogen, oxygen and nitrous oxide gases to form an oxidation layer over the second layer. A third layer of a conductive material is formed over the second layer to thereby form the capacitor. While the capacitor exhibits an improved leakage current reduction, overall capacitance is substantially unaffected, as compared to a similar capacitor having an oxidation layer built from a combination of
- 10 oxygen and hydrogen gases only.

FIG. 1

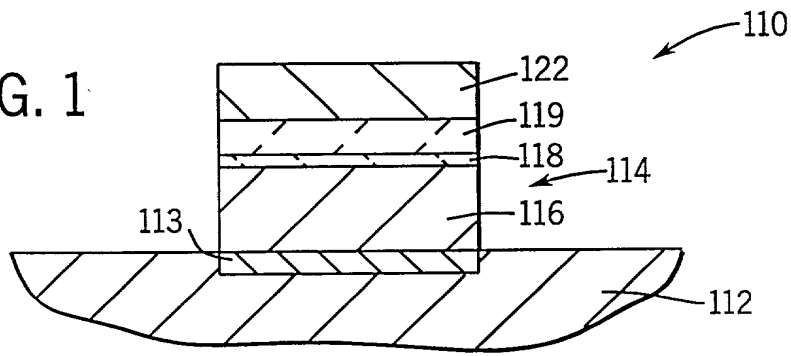


FIG. 2A

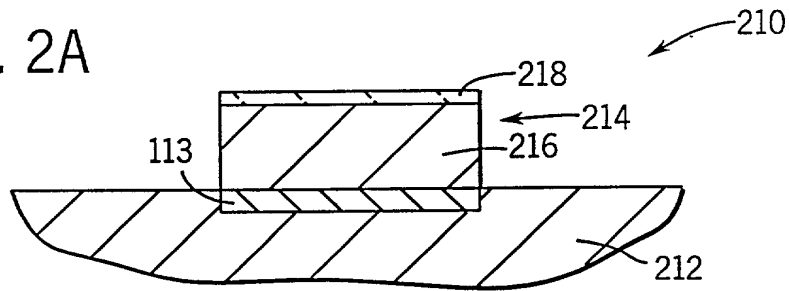


FIG. 2B

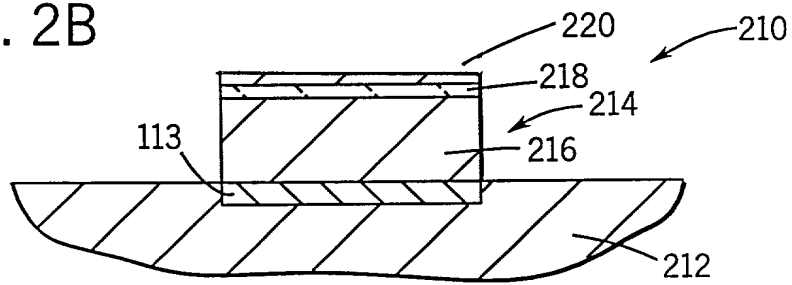


FIG. 2C

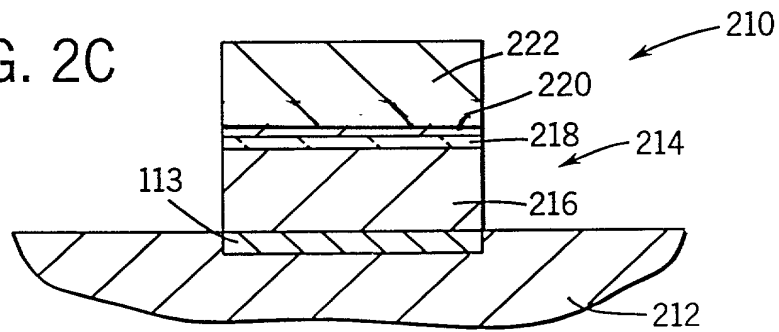


FIG. 3

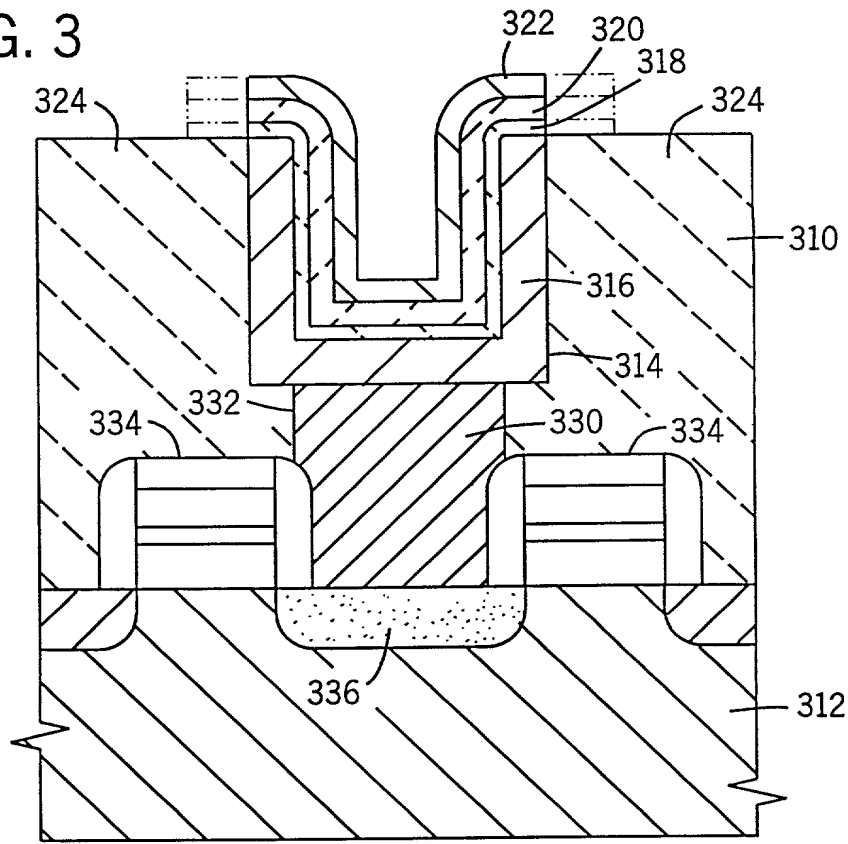
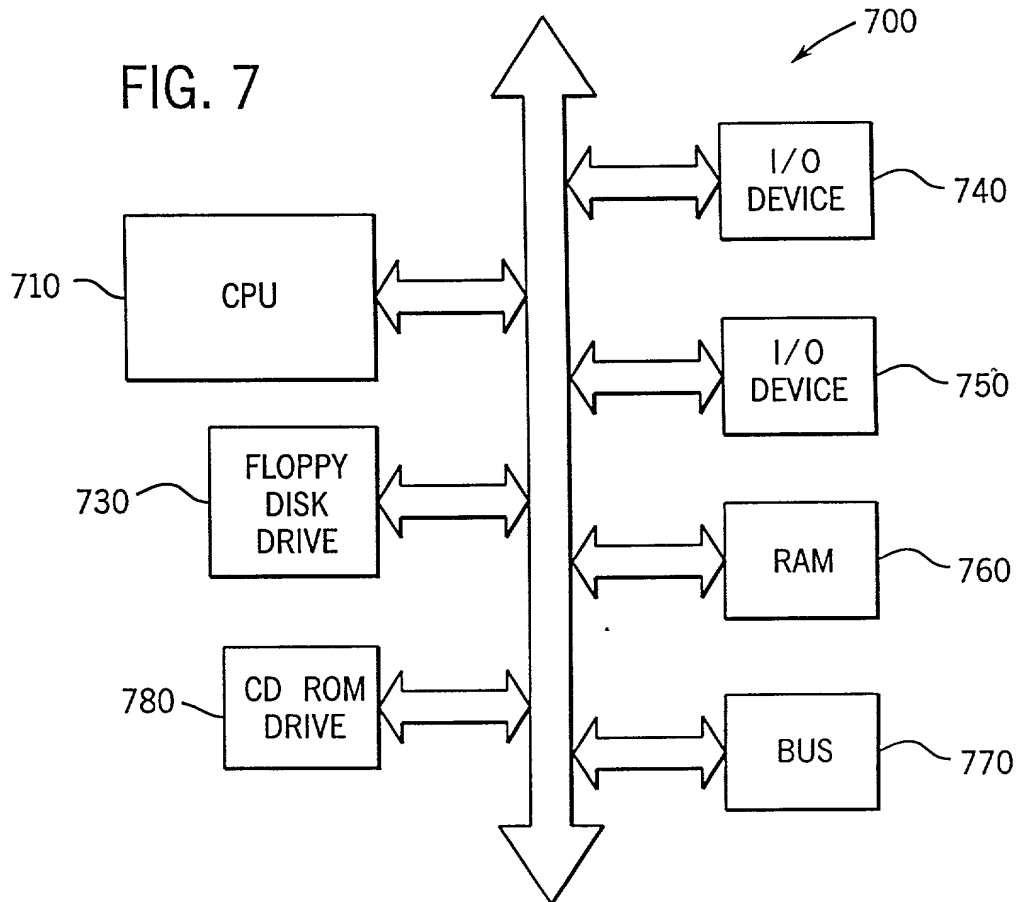


FIG. 7



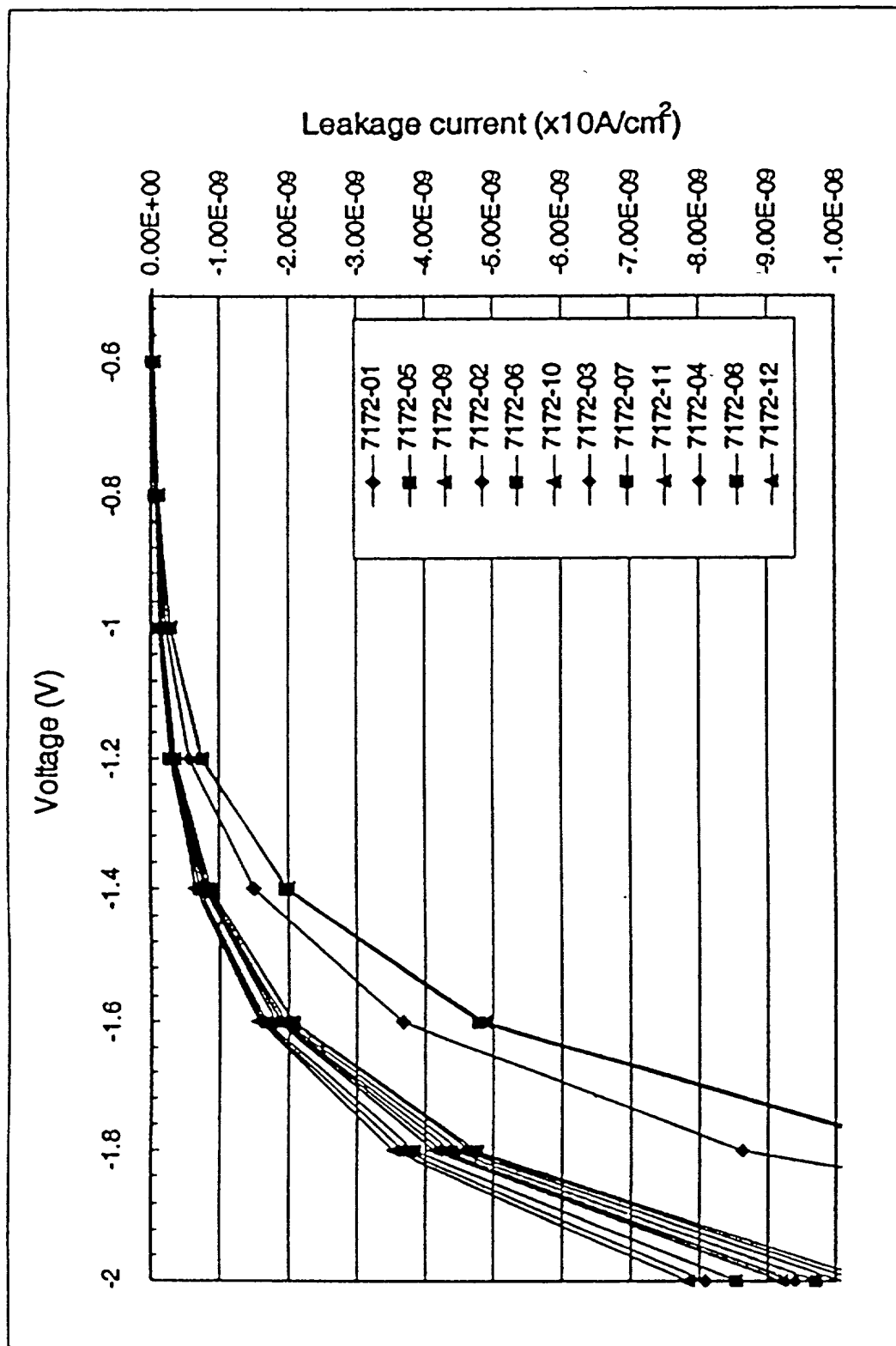


FIG. 4

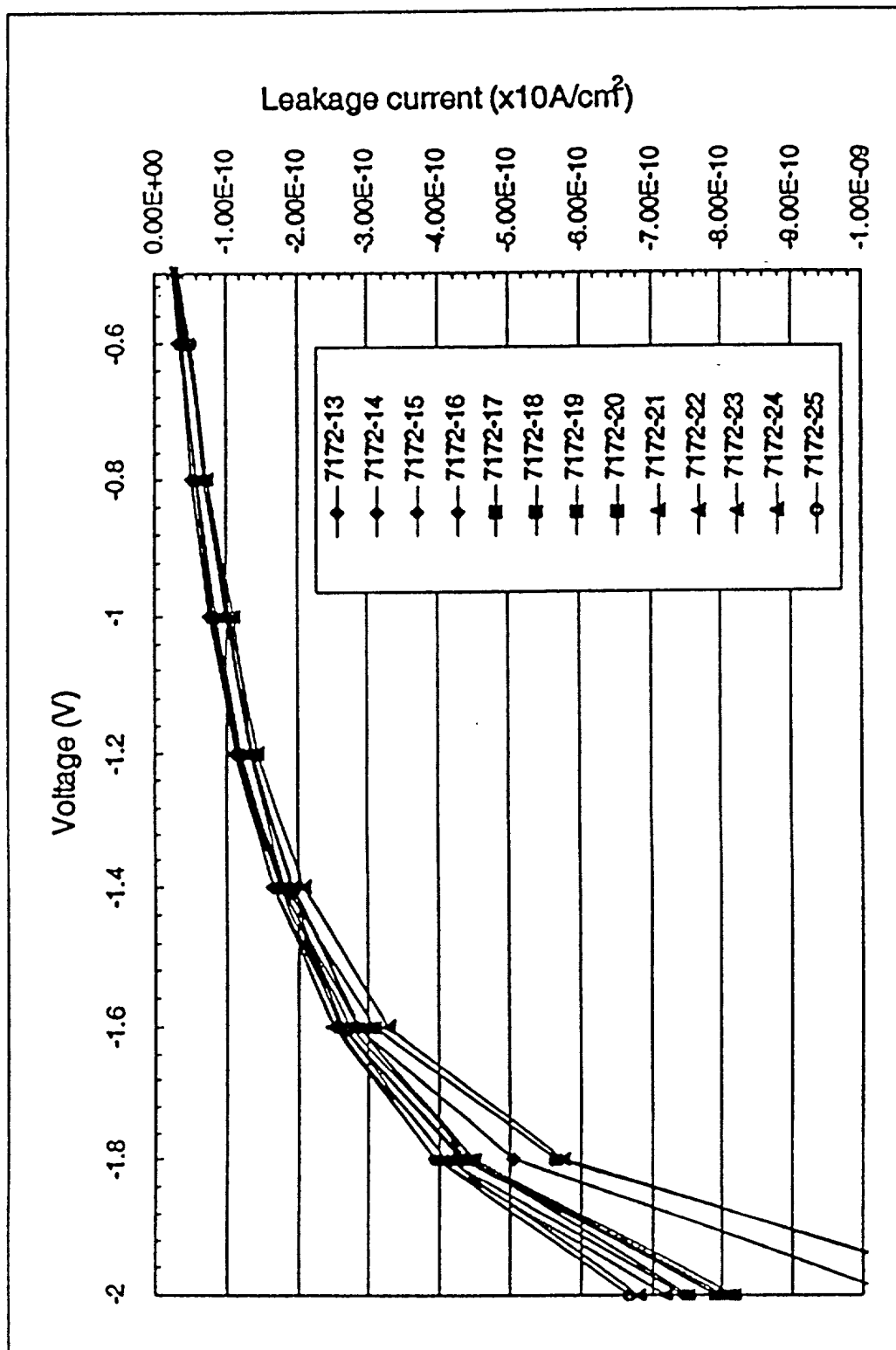


FIG. 5

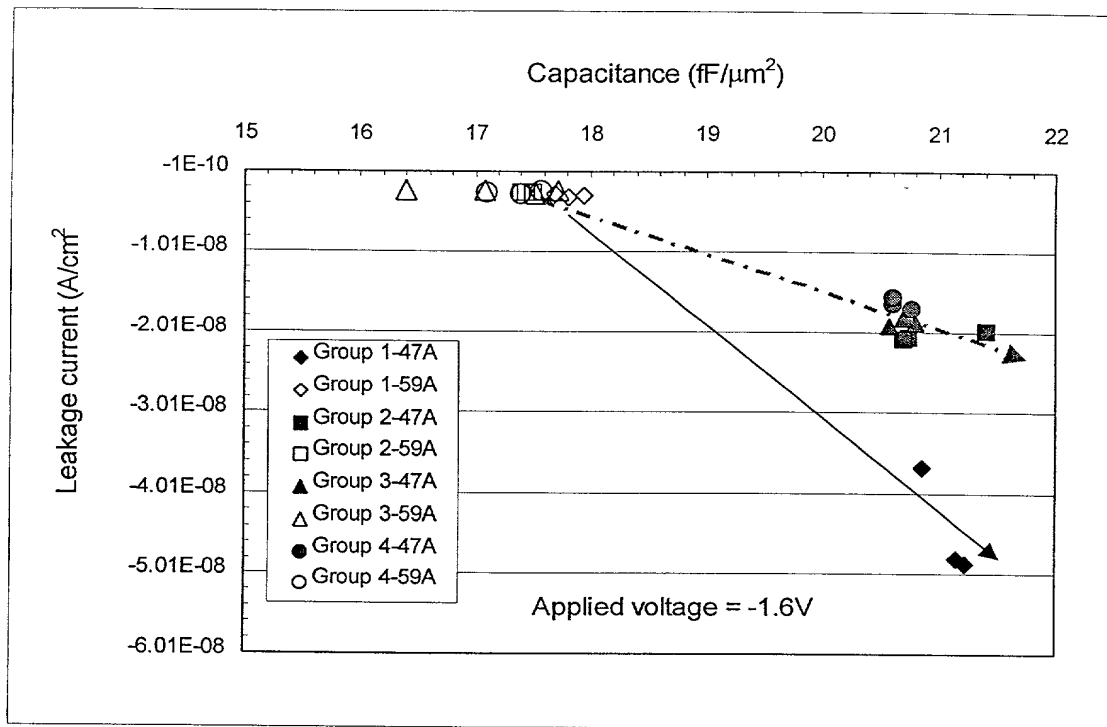


Figure 6.

Docket No.: M4065.0315/P315

Micron No.: 00-0135

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND STRUCTURE FOR REDUCING LEAKAGE CURRENT IN CAPACITORS

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Filing Date)	<input type="checkbox"/>
_____ (Number)	_____ (Country)	_____ (Filing Date)	<input type="checkbox"/>
_____ (Number)	_____ (Country)	_____ (Filing Date)	<input type="checkbox"/>

005109-0000

Docket No.: M4065.0315/P315

Micron No.: 00-0135

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

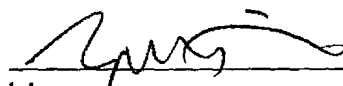
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Docket No.: M4065.0315/P315
Micron No.: 00-0135IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
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Inventor's signature:

Er-Xuan Ping

Date:

08/31/2000

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